REMARKS

Claims 1-7 and 9-30 are pending in the present application. In the Office Action, the Examiner objected to claims 5, 9-11, 24, and 26 because of various alleged informalities. Claims 5 and 9-11 have been amended to correct typographical errors. However, Applicants respectfully submit that claims 24 and 26 are correct in their present form. Applicants respectfully request that the Examiner's objections to claims 5, 9-11, 24, and 26 be withdrawn.

In the Office Action, claim 19 was rejected under 35 U.S.C. 102(e) as being anticipated by Nicholson (U.S. Patent No. 6,580,960). The Examiner's rejection is respectfully traversed.

Nicholson is concerned with finding combinations of operations and/or tools that may cause integration failure in semiconductor processing. Nicholson describes a failure signature analyzer 120 that determines a failure signature of a wafer processed in a semiconductor processing system 100 if a defect is found in the wafer. Nicholson also describes associating failure signatures of a number of wafers with various processing tools in order to determine combinations of the processing tools that are most likely to generate the failure signature. However, Nicholson is only concerned with identifying defects in individual wafers and appears to be completely silent with regard to <u>process drifts</u>.

Typically, <u>process drifts</u> are identified by comparing a plurality of measurements to a target value. For example, the third and/or forth "Western Electric rules" may be used to identify a process drift (Western Electric Rule 3: Four out of five consecutive measurements exceed one standard deviation from the target on one side of the target, *i.e.*, $4/5 > \sigma$. Western Electric Rule 4: Eight consecutive measurement points on one side of the target.) See Patent Application, page 4, ll. 10-14. The conditions set forth in the Western Electric rules for identifying a process drift do not require any kind of failure and/or defect in the processed wafer. For example, one indication

of a failure or a defect associated with a wafer is given by Western Electric rule 1, which states that one measurement exceeds three standard deviations from the target (*i.e.*, $1>3\sigma$). See Patent Application, page 10, ll. 8-9. Thus, Applicants respectfully submit that Nicholson fails to teach or suggest identifying manufactured items associated with <u>a process drift</u>.

For at least the aforementioned reasons, Applicants respectfully submit that claim 19 is not anticipated by Nicholson and request that the Examiner's rejection of this claim under 35 U.S.C. 102(e) be withdrawn.

In the Office Action, claims 1-2, 6-7, 9-13, 17-18, and 20-23 were rejected under 35 U.S.C. § 103(a) as being obvious over Nicholson in view of Milor (United States Patent No. 5,886,909). The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka,* 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). In addition, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997).

As discussed above, Applicants respectfully submit that Nicholson fails to teach or suggest identifying manufactured items associated with <u>a process drift</u>. Consequently, Applicants respectfully submit that Nicholson also fails to teach or suggest comparing the characteristic threads for at least those manufactured items associated with the <u>process drift</u> and

determining at least one potential cause for the process drift based on the comparison of the characteristic threads. Milor describes a simulation technique that may be used to diagnose defects in individual integrated circuit wafers but is similarly silent with regard to process drifts.

Furthermore, Applicants respectfully submit that the cited references provide no suggestion or motivation to modify the prior art to arrive at Applicants claimed invention. Nicholson and Milor are entirely concerned with detecting and/or diagnosing defects on a single wafer. As discussed above, an analysis of measurement trends (which are not necessarily associated with or indicative of faults or defects) across multiple wafers is typically used to identify a process drift. Accordingly, these references provide no suggestion or motivation for identifying a process drift.

As discussed in a previous response, Applicants also submit that the cited references do not describe or suggest generating a plurality of characteristic threads based on the production environment data, at least one of the characteristic threads being associated with other than processing tools used in the process flow. The Examiner admits that Nicholson does not teach or suggest at least one characteristic thread associated with other than processing tools used in the process flow. To remedy this admitted deficiency in the primary reference, the Examiner alleges that Milor teaches the missing limitation and that it would be obvious to combine the teachings of Milor and Nicholson to arrive at Applicants' claimed invention. Applicants respectfully disagree for at least the following reasons.

Milor describes simulating defect profiles associated with bubbles in a photoresist layer. The defect profiles may be stored and later used for comparison with actual measured wafer profiles. See Milor, col. 6, ll. 9-11. However, Milor does not teach or suggest forming a characteristic thread using either the simulated defect profiles or the individual measured wafer

defects. To the contrary, Milor appears to be completely silent with regard to characteristic threads. Accordingly, Applicants respectfully submit that Milor fails to teach or suggest, or provide any motivation for, <u>at least one characteristic thread associated with other than processing tools used in the process flow</u>.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Nicholson and Milor, either alone or in combination. Applicants respectfully request that the Examiner's rejections of claims 1-2, 6-7, 9-13, 17-18, and 20-23 under 35 U.S.C. 103(a) be withdrawn.

In the Office Action, the Examiner indicated that the claims 3-5, 14-16, and 30 are allowed. The Examiner also indicated that claims and that claims 24-29 were objected to as being dependent upon a rejected base claim but that these claims included allowable subject matter. In view of the aforementioned arguments, Applicants respectfully submit that claims 24-29 are in condition for allowance and request that the Examiner's objections to these claims be withdrawn.

In view of the remarks set forth herein, the application is believed to be in condition for allowance and notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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